DATA SHEET

UMA1022M
Low cost dual frequency synthesizer for radio telephones

Preliminary specification
Supersedes data of 1996 Oct 02
File under Integrated Circuits, IC17

1998 May 15

Philips Semiconductors

PHILIPS

Low cost dual frequency synthesizer for radio telephones

UMA1022M

FEATURES

- Low phase noise
- Low current from 3 V supply
- Fully programmable dividers
- 3-line serial interface bus
- Input reference buffer configurable as an oscillator with external crystal resonator
- Wide compliance voltage charge pump outputs
- Two power-down input control pins.

APPLICATIONS

- 900 MHz and 2 GHz digital radio telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1022M BICMOS device integrates prescalers, programmable dividers, a crystal oscillator/buffer and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd or a single LiIon cell in pocket phones, or from an external 3 V supply.

The synthesizers operate at RF input frequencies up to 2.1 GHz and 550 MHz. All divider ratios are supplied via a 3-wire serial programming bus. The reference divider uses a common, fully programmable part and a separate subdivider section. In this way the comparison frequencies are related to each other allowing optimum isolation between charge pump pulses.

Separate power and ground pins are provided to the analog (charge pump, prescaler) and digital (CMOS) circuits. An independent supply for the crystal oscillator section allows maximum frequency stability. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD} and V_{DDX} must be at the same potential. V_{CCA} and V_{CCB} must be equal to each other and equal to or greater than V_{DD} (e.g. V_{DD} = 3 V and V_{CCA} = 4 V for wider VCO control voltage range).

The charge pump currents (phase detector gain) are fixed by internal resistances and controlled by the serial interface. Only passive loop filters are necessary; the charge pumps function within a wide voltage compliance range to improve the overall system performance.

Suitable pin layout is chosen to minimize coupling and interference between signals entering or leaving the chip.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1022M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	$V_{CCA} = V_{CCB} \geq V_{DD}$	2.7	3.0	4.0	V
V_{CCA}, V_{CCB}	analog supply voltages	$V_{CCA} = V_{CCB} \geq V_{DD}$	2.7	3.0	4.0	V
V_{DDX}	crystal reference supply voltage	$V_{DDX} = V_{DD}$	2.7	3.0	4.0	V
I_{tot}	all supply currents ($I_{DD} + I_{CCA} + I_{CCB} + I_{DDX}$) in active mode	$\overline{E}$ = 1; $V_{CCA} = V_{CCB}$ = 3.0 V; $V_{DDX} = V_{DD}$ = 3.0 V;				
		XON = 0	–	14.65	–	mA
		XON = 1	–	15.9	–	mA
$I_{tot(pd)}$	total supply currents in power-down mode		–	40	–	µA
f_{RF}	RF input frequency		300	–	2100	MHz
f_{IF}	IF input frequency		50	–	550	MHz
f_{xtal}	crystal reference oscillator frequency		3	–	25	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

BLOCK DIAGRAM

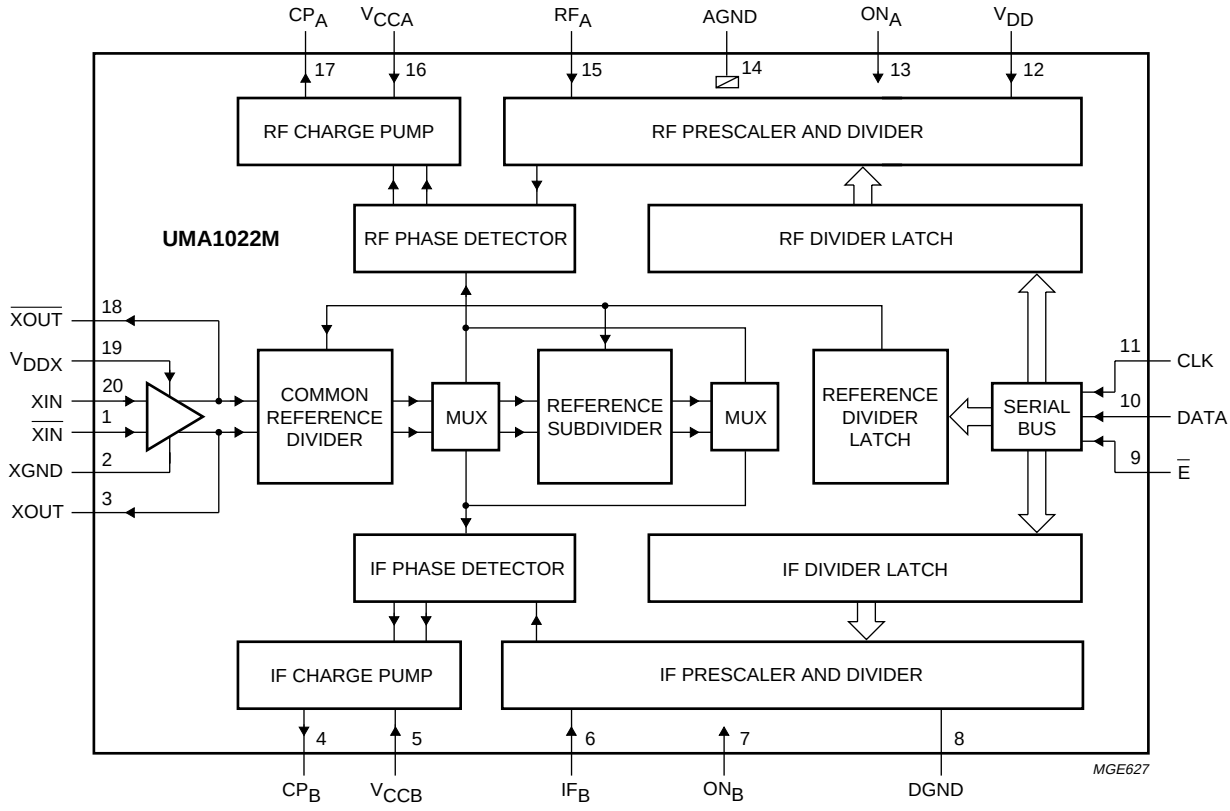


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{XIN}$	1	inverting crystal reference input
XGND	2	ground for crystal oscillator circuits
XOUT	3	crystal oscillator buffer output
CP_B	4	IF synthesizer charge pump output
V_{CCB}	5	analog supply to IF synthesizer
IF_B	6	IF VCO main divider input
ON_B	7	IF power-on input; ON_B = HIGH means IF synthesizer is active
DGND	8	digital circuits ground
$\overline{E}$	9	programming bus enable input
DATA	10	programming bus data input
CLK	11	programming bus clock input
V_{DD}	12	digital circuits supply voltage
ON_A	13	RF power-on input; ON_A = HIGH means RF synthesizer is active
AGND	14	analog circuits ground
RF_A	15	RF VCO main divider input
V_{CCA}	16	analog supply to RF synthesizer
CP_A	17	RF synthesizer charge pump output
$\overline{XOUT}$	18	inverting oscillator buffer output
V_{DDX}	19	supply voltage to crystal oscillator circuits
XIN	20	non-inverting crystal reference input

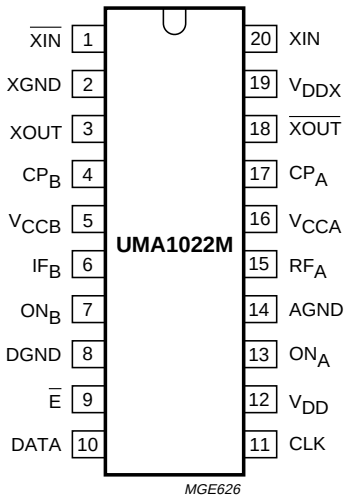


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main dividers

The main dividers are clocked at pin RF_A by the RF oscillator signal and at pin IF_B by the IF oscillator signal. The inputs are AC coupled through external capacitors. Input impedances are high, dominated by parasitic package capacitances, so matching is off-chip.
The sensitive dividers operate with signal levels from 35 to 225 mV (RMS), at frequencies up to 2.1 GHz (RF part) and up to 550 MHz (IF part). Both include programmable bipolar prescalers followed by CMOS counters. The RF main divider allows programmable ratios from 512 to 65535; the IF blocks accept values between 128 and 16383.

Crystal oscillator

A fully differential low-noise amplifier/buffer is integrated providing outputs to drive other circuits, and to build a crystal oscillator; only needed are an external resonance circuit and tuning elements (temperature compensation). A bus controlled power-down mode disables the low-noise amplifier to reduce current if not needed.

The normal differential input pins drive a clock buffer to provide edges to the programmable reference divider at frequencies up to 25 MHz. The inputs are AC coupled through external capacitors, and operate with signals down to 35 mV (RMS) and up to 0.5 V (RMS).

Various crystal oscillator structures can be built using the amplifier. By coupling one output back to the appropriate input through the resonator, and decoupling the other input to ground, the second output becomes available to deliver the reference frequency to other circuits.

Reference dividers

A first common divider circuit produces an output frequency for RF or IF synthesizer phase comparison, depending on the P/A bit. It drives a second independent divider, which delivers the reference edge to the IF or RF synthesizer phase comparator. When P/A is logic 1, the output of the subdivider is connected to the RF phase comparator, whereas the output of the common divider is connected to the IF phase detector.

The phase comparators run at related frequencies with a controlled phase difference to avoid interference when in-lock. The common 10-bit section permits divide ratios from 8 to 1023; the second subdivider allows phase comparison frequency ratios between 1 and 16. Table 2 indicates how to program the corresponding bits to get the wanted ratio.

Phase comparators

The phase detectors are driven by the output edges selected by the main and reference dividers. Each generates lead and lag signals to control the appropriate charge pump. The pumps output current pulses appear at pins CP_A (RF synthesizer) and CP_B (IF synthesizer). The current pulse duration is at least equal to the difference in time of arrival of the edges from the two dividers. If the main divider edge arrives first, CP_A or CP_B sink current. If the reference divider edge arrives first, CP_A or CP_B source current. For correct PLL operation the VCOs need to have a positive frequency/voltage control slope.

The currents at CP_A and CP_B are programmed via the serial bus as multiples of an internally-set reference current. The passage into power-down mode is synchronized with respect to the phase detector to prevent output current pulses being interrupted. Additional circuitry is included to ensure that the gain of the phase comparators remains linear even for small phase errors.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, clock (CLK) and enable ($\overline{E}$). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns HIGH. During normal operation, $\overline{E}$ should be kept HIGH. Only the last 19 bits serially clocked into the device are retained within the programming register.

Additional leading bits are ignored, and no check is made on the number of clock pulses. The NMOS-rich design uses virtually no current when the bus is inactive; power-up is initiated when enable is taken LOW, and power-down occurs a short time after enable returns HIGH. Bus activity is allowed when either synthesizer is active or in power-down (ON_A and ON_B inputs LOW) mode. Fully static CMOS registers retain programmed data whatever the power-down state, as long as the supply voltage is present.

Data format

The leading bits (dt15 to dt0) make up the data field, while the trailing three bits (ad2 to ad0) comprise an address field. The UMA1022M uses 4 of the 8 available addresses. The data format is shown in Table 1. The first bit entered is dt15, the last bit is ad0. For the divider ratios, the first bits entered (P0 and R0) are the Least Significant Bits (LSB). **This is different from previous Philips synthesizers.**

The trailing address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch. To avoid erroneous divider ratios, the load pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer.The test register bits should not normally be programmed active (HIGH); normal operation requires them set LOW. When the supply voltage is established an internal power-up initialization pulse is generated to preconfigure the circuit state. Production testing does not verify that all bits are preconfigured correctly.

Power-down mode

The RF and IF synthesizers are **on** when respectively the input signal ON_A and ON_B are HIGH. When turned **on**, the dividers and phase detector are synchronized to avoid random phase errors. When turned **off**, the phase detector is synchronized to avoid interrupting charge pump pulses. The UMA1022M has a very low current consumption in the power-down mode.

Table 1 Bit allocation; note 1

FIRST IN						REGISTER BIT ALLOCATION									LAST IN			
DATA FIELD																ADDRESS		
dt15	**dt14**	**dt13**	**dt12**	**dt11**	**dt10**	**dt9**	**dt8**	**dt7**	**dt6**	**dt5**	**dt4**	**dt3**	**dt2**	**dt1**	**dt0**	**ad2**	**ad1**	**ad0**
Test bits(2)				CPI	S/D	XON(3)	X	X	X	X	P/A(4)	REFDIV2(5)				0	1	1
P0(6)	RF synthesizer main divider coefficient														P15	0	0	0
X	X	X	X	X	X	R0(6)	reference divider coefficient								R9	0	0	1
X	X	A0(6)	IF synthesizer main divider coefficient												A13	0	1	0

Notes

1. X = don't care.
2. The test bits (at address 011) should not be programmed with any other value except all zeros for normal operation.
3. Bit XON = power-on of crystal oscillator low-noise amplifier; logic 1 turns **on** circuit block.
4. Bit P/A = 1 selects the output of the reference subdivider to the RF synthesizer and the output of the common reference divider to the IF synthesizer.
5. The coefficient REFDIV2 (4 bits) selects the phase comparison ratio (1 to 16) between IF and RF synthesizers (see Table 2).
6. P0 is the LSB of the RF main divider coefficient; R0 is the LSB of the reference divider coefficient; A0 is the LSB of the IF main divider.

Table 2 Programming the coefficient REFDIV2 for reference subdivider

dt3 (LSB)	dt2	dt1	dt0 (MSB)	REFDIV2
0	0	0	0	1
1	0	0	0	2
0	1	0	0	3
1	1	0	0	4
0	0	1	0	5
1	0	1	0	6
0	1	1	0	7
1	1	1	0	8
0	0	0	1	9
1	0	0	1	10
0	1	0	1	11
1	1	0	1	12
0	0	1	1	13
1	0	1	1	14
0	1	1	1	15
1	1	1	1	16

Table 3 RF and IF synthesizer nominal charge pump currents (gain)

CPI	SINGLE/DOUBLE	I_{CPA} (μA)	I_{CPB} (μA)
0	0	470	470
0	1	840	840
1	0	1410	470
1	1	2480	840

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}, V_{DDX}	digital and crystal reference supply voltages	–0.3	+5.5	V
V_{CCA}, V_{CCB}	analog charge pump supply voltages	–0.3	+5.5	V
$V_C - V_D$	difference in voltage between analog and digital supplies	–0.3	+5.5	V
V_n	voltage			
	at pins 7, 9, 10, 11 and 13	–0.3	V_{DD} + 0.3	V
	at pins 1, 3, and 20	–0.3	V_{DDX} + 0.3	V
	at pins 4 and 6	–0.3	V_{CCB} + 0.3	V
	at pins 15 and 17	–0.3	V_{CCA} + 0.3	V
ΔV_{GND}	difference in voltage between any of DGND, AGND and XGND (these pins should be connected together)	–0.3	+0.3	V
P_{tot}	total power dissipation	–	110	mW
T_{stg}	IC storage temperature	–55	+125	°C
T_{amb}	operating ambient temperature	–30	+85	°C
$T_{j(max)}$	maximum junction temperature	–	150	°C

HANDLING

All pins withstand class 1 ESD test in accordance with *"EIA/JESD22-A114-A"* electrostatic discharge (ESD) sensitivity testing Human Body Model (HBM).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit; T_{amb} = 25 °C; $V_{DD} = V_{DDX}$ = 2.7 to 4.0 V; $V_{CCA} = V_{CCB}$ = 2.7 to 4.0 V; $V_{CCA} = V_{CCB} \geq V_{DD}$; unless otherwise specified. Characteristics for which only a typical value is given are not tested.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; pins 5, 12, 16 and 19						
V_{DD}, V_{DDX}	digital and crystal reference supply voltages	$V_{DD} = V_{DDX}$; $V_{CCA} = V_{CCB} \geq V_{DD}$	2.7	3.0	4.0	V
V_{CCA}, V_{CCB}	charge pump supply voltages	$V_{CCA} = V_{CCB} \geq V_{DD}$	2.7	3.0	4.0	V
I_{DD}	synthesizer digital supply current	V_{DD} = 3 V; $\overline{E}$ = 1; ON_A and ON_B = 1	–	1.5	2.1	mA
I_{DDX1}	reference block supply current	V_{DDX} = 3 V; XON = 0	–	0.25	0.4	mA
I_{DDX2}	crystal oscillator and buffer currents	V_{DDX} = 3 V; XON = 1	–	1.5	1.8	mA
I_{CCA}	RF synthesizer charge pump and prescaler supply currents	V_{CCA} = 3 V; ON_A and ON_B = 1	–	8.1	9.8	mA
I_{CCB}	IF synthesizer charge pump and prescaler supply currents	V_{CCB} = 3 V; ON_A and ON_B = 1	–	4.8	5.7	mA
$I_{tot(pd)}$	total supply currents ($I_{CCA(pd)} + I_{DD(pd)} + I_{CCB(pd)} + I_{DDX(pd)}$) in power-down mode	$\overline{E} = V_{DD}$; CLK and DATA = 0 V or V_{DD}; ON_A and ON_B = 0; XON = 0	–	40	80	µA
RF main divider input; pin 15						
f_{RF}	RF input frequency		300	–	2100	MHz
$V_{RF(rms)}$	AC-coupled input signal level (RMS value)	f_{RF} = 600 to 2100 MHz	35	–	225	mV
		f_{RF} = 300 to 600 MHz	70	–	225	mV
R_m	main divider ratio		512	–	65535	
Z_i	input impedance (real part)	f_{RF} = 2 GHz	–	60	–	Ω
C_i	pin input capacitance		–	2	–	pF
IF main divider input; pin 6						
f_{IF}	IF input frequency		50	–	550	MHz
$V_{IF(rms)}$	AC-coupled input signal level (RMS value)	f_{IF} = 150 to 550 MHz	35	–	225	mV
		f_{IF} = 100 to 150 MHz	50	–	225	mV
		f_{IF} = 50 to 100 MHz	100	–	225	mV
R_m	main divider ratio		128	–	16383	
Z_i	input impedance (real part)	f_{IF} = 400 MHz	–	60	–	Ω
C_i	pin input capacitance		–	2	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Synthesizers reference divider input; pins 1 and 20						
f_{xtal}	crystal reference oscillator frequency		3	–	25	MHz
$V_{xtal(rms)}$	sinusoidal input signal level between pins 1 and 20 (RMS value)	single-ended;				
		f_{xtal} = 6 to 25 MHz	35	–	250	mV
		f_{xtal} = 3 to 6 MHz	70	–	250	mV
		differential;				
		f_{xtal} = 6 to 25 MHz	70	–	500	mV
		f_{xtal} = 3 to 6 MHz	140	–	500	mV
R_{refc}	common reference division ratio		8	–	1023	
R_{refa}	reference subdivider division ratio		1	–	16	
Z_i	input impedance (real part) per pin	f_{xtal} = 10 MHz; XON = 1	–	4	–	kΩ
C_i	typical pin input capacitance		–	2	–	pF
NF	small signal differential input noise figure	matched to a 4 kΩ source; XON = 1	–	4.5	–	dB
Phase detectors						
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
Charge pump outputs; pins 4 and 17						
V_{CPA}	output voltage compliance range; RF synthesizer		0.4	–	V_{CCA} – 0.4	V
V_{CPB}	output voltage compliance range; IF synthesizer		0.4	–	V_{CCB} – 0.4	V
$I_{ocp(err)}$	charge pump output current error	note 1	–25	–	+25	%
I_{match}	sink-to-source current matching		–	±5	–	%
I_{Lcp}	charge pump **off** leakage current	V_{CPA} = ½V_{CCA}; V_{CPB} = ½V_{CCB}	–5	±1	+5	nA
Phase noise						
N_{900}	RF synthesizer's contribution to close-in phase noise of 0.9 GHz VCO signal inside closed-loop bandwidth	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 200 kHz	–	–86	–	dBc/Hz
N_{1800}	RF synthesizer's contribution to close-in phase noise of 1.8 GHz VCO signal inside closed-loop bandwidth	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 200 kHz	–	–80	–	dBc/Hz
N_{180}	IF synthesizer's contribution 180 MHz VCO signal inside closed-loop bandwidth	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 1000 kHz	–	–104	–	dBc/Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Interface logic input signal levels; pins 7, 9, 10, 11 and 13						
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	μA
C_i	input capacitance		–	2	–	pF
Low noise crystal oscillator amplifier output signals; pins 3 and 18						
Z_o	differential output impedance (real part)	f_{xtal} = 10 MHz	–	2	–	kΩ
V_{XOUT}, V_{XOUTN}	DC output voltage		–	2.29	–	V
$G_{v(diff)}$	small signal differential voltage gain	XON = 1; f_{xtal} = 10 MHz	18	20	22	dB
$V_{o(p-p)}$	limiting differential output voltage swing (peak-to-peak value)	XON = 1	–	2	–	V
$\Delta f/f(V_{DDX})$	frequency stability as a function of supply voltage change (referenced to initial frequency)	V_{DDX} = 3 V ±5%; note 2	–	±0.25	–	ppm
System specification						
$FTRF_{IF}$	RF frequency and close harmonics feedthrough to IF frequency	note 3	–	70	–	dBc
$FTIF_{RF}$	IF frequency and close harmonics feedthrough to RF frequency	note 3	–	50	–	dBc

Notes

1. Conditions: $0.4 < V_{CPA} < (V_{CCA} - 0.4)$ and $0.4 < V_{CPB} < (V_{CCB} - 0.4)$.
2. This value is directly dependent on the external resonator quality factor. Only guaranteed for the application circuit which is given in Fig.5.
3. Only guaranteed on the Philips application board.

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{DDX} = V_{CCA} = V_{CCB} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	100	–	–	ns
t_{END}	delay from last falling clock edge	20	–	–	ns
$t_{W(min)}$	minimum inactive pulse width	1500(1)	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width ($t_{W(min)}$) can be smaller than 1.5 µs when the following conditions are fulfilled:

   a) Main divider input frequency $f_{RF} > \frac{383}{t_{W(min)}}$

   b) Reference divider input frequency $f_{xtal} > \frac{3}{t_{W(min)}}$

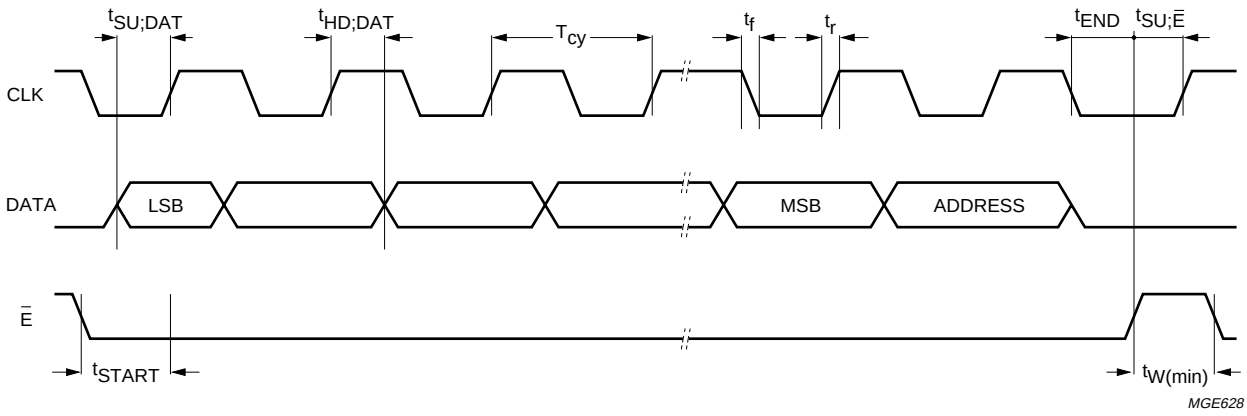


Fig.3 Serial bus timing diagram.

AC TIMING CHARACTERISTICS

$V_{DD} = V_{DDX} = V_{CCA} = V_{CCB} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{PUP}	delay for initial power-up	–	400	–	µs
t_{PDWN}	time for power-down from $\overline{E} = 0$ ($ON_A/ON_B = 0$)	–	100	–	µs
t_{START}	time to turn-on either the RF or IF synthesizer from ON_A/ON_B	–	50	–	µs
t_{END}	time to turn-off either the RF or IF synthesizer from ON_A/ON_B	–	70	–	µs
t_{SEND}	waiting time before sending data on the serial bus	15000	–	–	µs

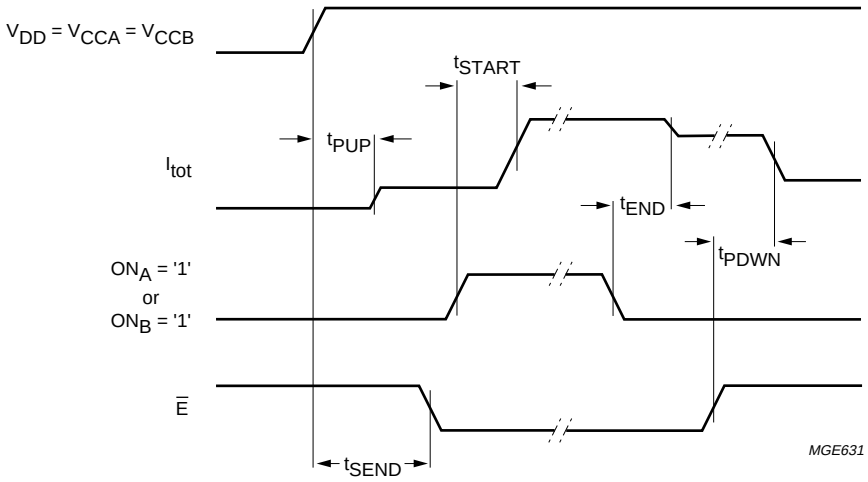
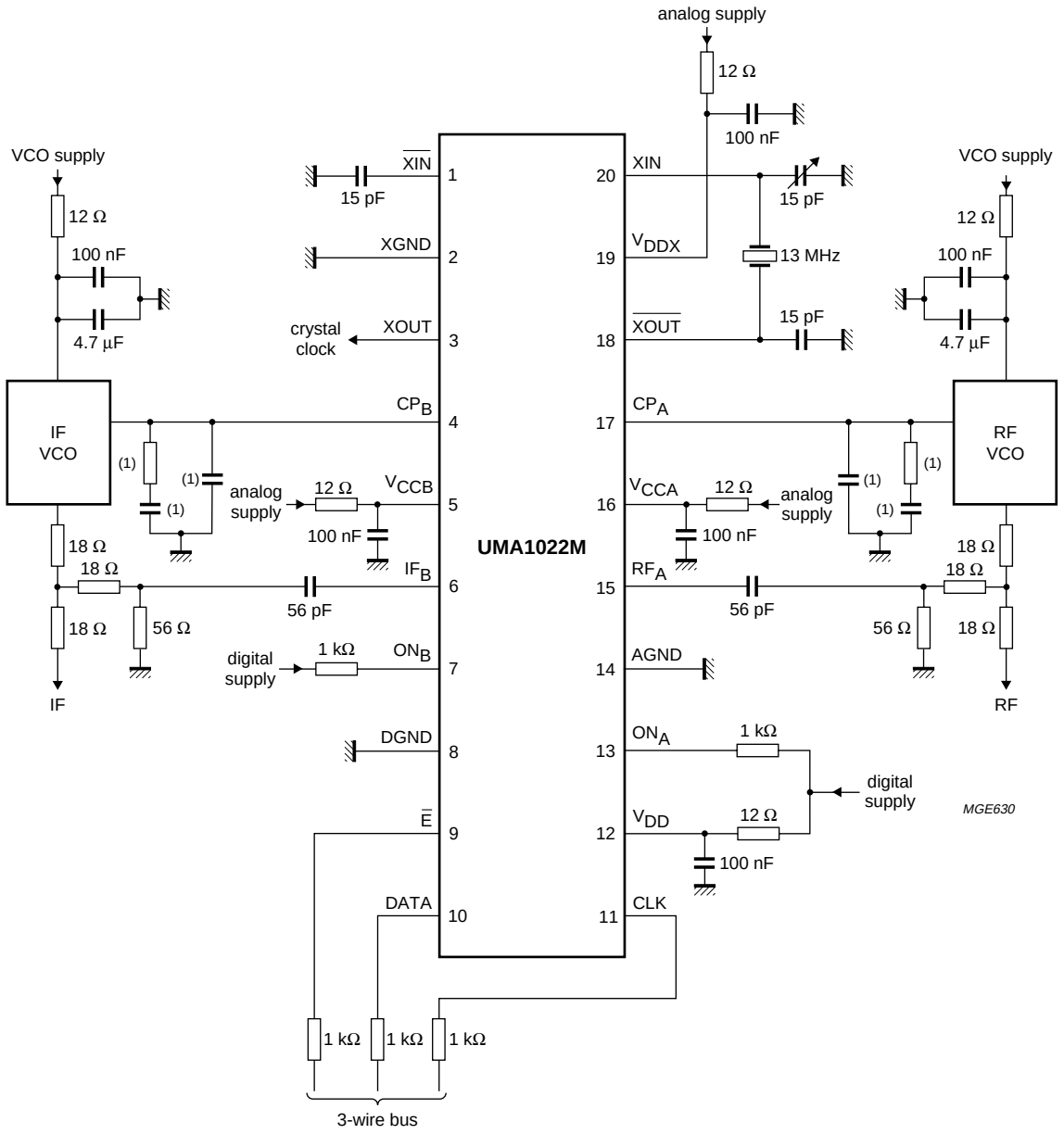


Fig.4 AC timing characteristics.

APPLICATION INFORMATION



(1) Loop filter values depend on the application.

Fig.5 Typical test and application diagram.

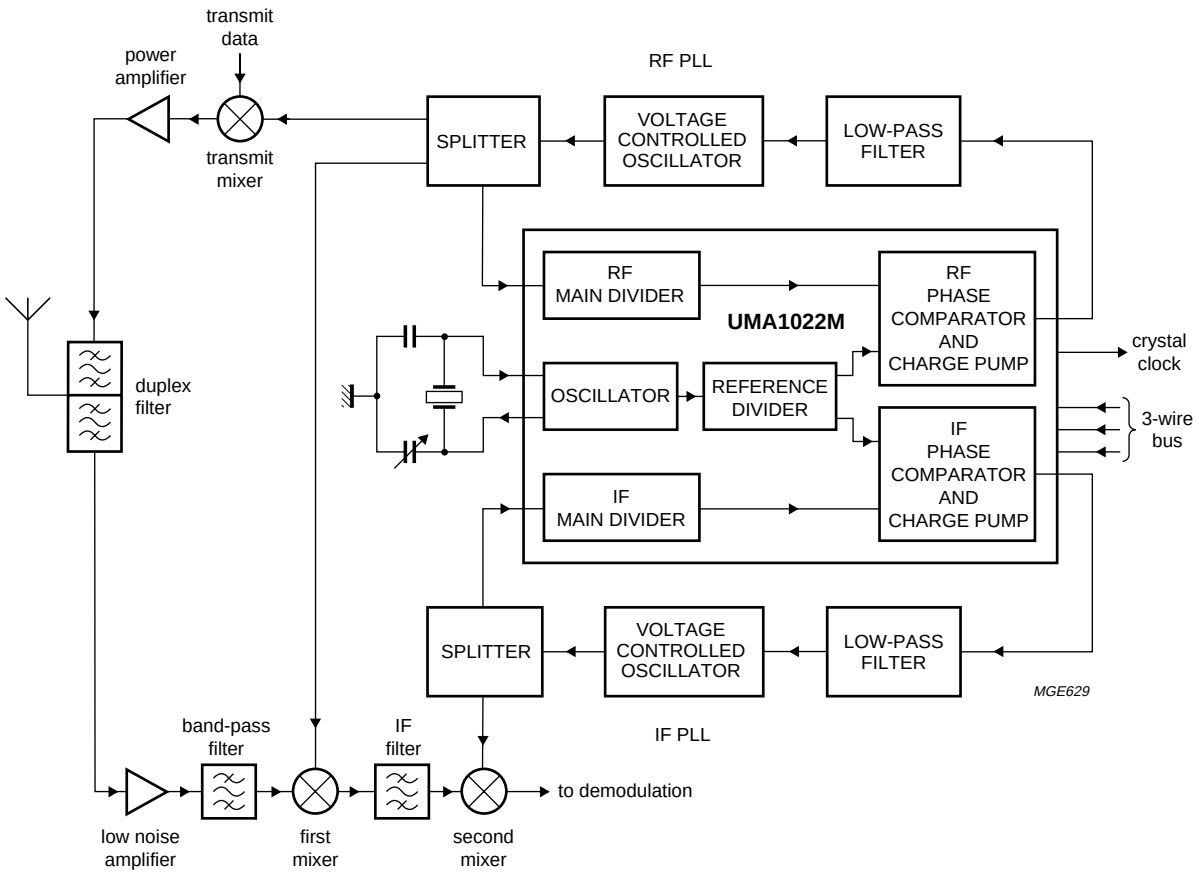
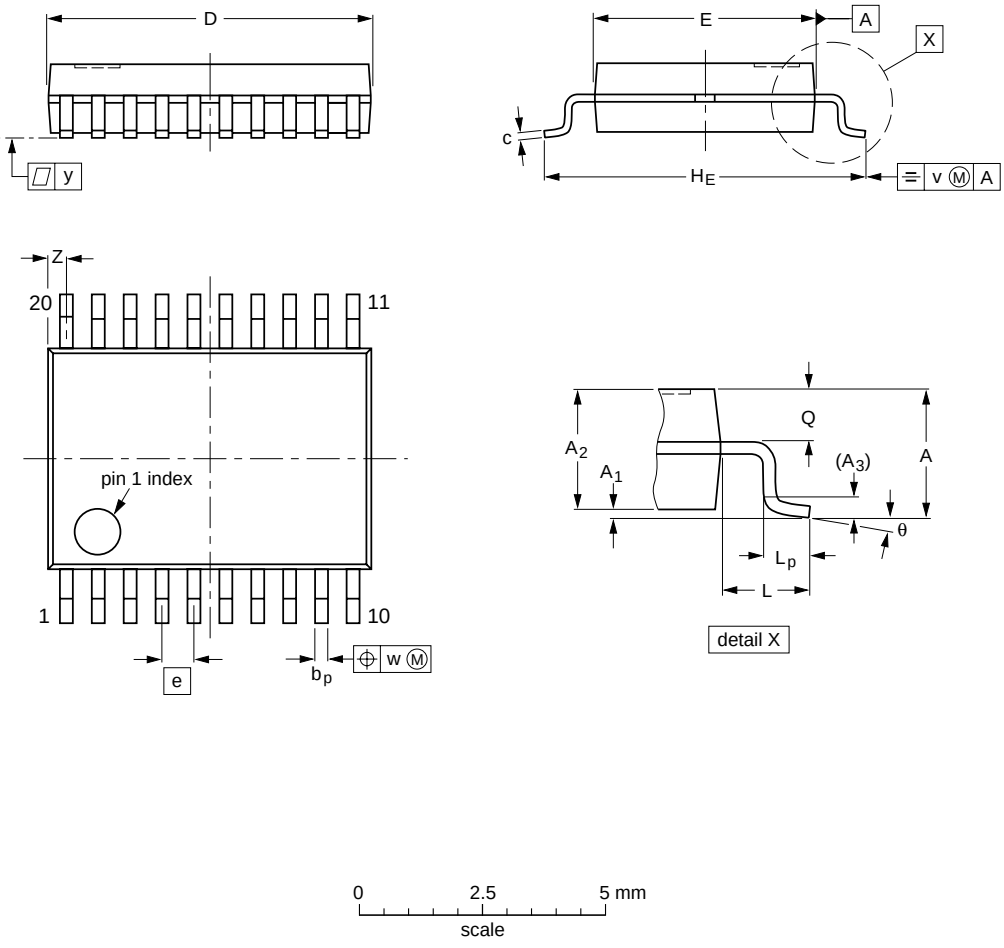


Fig.6 Application block diagram.

PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

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